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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/778,495	02/07/2001	Marquette John Anderson	TI-30831	8073
23494	7590	07/01/2008	EXAMINER	
TEXAS INSTRUMENTS INCORPORATED			CHANKONG, DOHM	
P O BOX 655474, M/S 3999				
DALLAS, TX 75265			ART UNIT	PAPER NUMBER
			2152	
			NOTIFICATION DATE	DELIVERY MODE
			07/01/2008	ELECTRONIC

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JOHN MARQUETTE ANDERSON and HAKIM BEDERR

Appeal 2008-0624
Application 09/778,495
Technology Center 2100

Decided: June 27, 2008

Before JAMES D. THOMAS, JAY P. LUCAS, and
ST. JOHN COURTENAY III, *Administrative Patent Judges*.

COURTENAY, *Administrative Patent Judge*.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 1-20. We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM IN PART.

THE INVENTION

The disclosed invention relates generally to integrated circuits. More particularly, Appellants' invention is directed to a multiprocessor system verification circuit (Spec. 1).

Independent claims 1 and 8 are illustrative:

1. A processing device comprising:
 - a master processor;
 - a system memory;
 - a slave processor subsystem including:
 - a slave processor;
 - a shared memory accessible by said master processor and said slave processor;
 - an external memory interface allowing said slave processor to access said system memory;
 - circuitry for receiving a signal for specifying a normal mode for normal operation of the processing device or verification mode for testing the processing device; and
 - a verification interface for selectively passing system memory accesses either to the system memory or the shared memory responsive to the signal, wherein accesses directed towards the system memory access are passed to said system memory in a normal mode and

wherein accesses directed towards the system memory are passed to said shared memory in a verification mode.

8. A method of verification of a processing device including a master processor subsystem having a master processor and a system memory and a slave processor subsystem having a slave processor, a external memory interface for accessing said system memory, and a shared memory accessible by the master processor and slave processor, comprising the steps of:

receiving a signal for specifying a normal mode for normal operation of the processing device or a verification mode for testing the processing device;

selectively passing system memory accesses to said system memory in a normal mode; and

selectively passing system memory accesses to said shared memory in a verification mode.

THE REFERENCES

The Examiner relies upon the following references as evidence in support of the rejections:

Baxter	US 5,887,146	Mar. 23, 1999
Corrigan	US 6,016,525	Jan. 18, 2000
DeRoo	US 6,161,162	Dec. 12, 2000

THE REJECTIONS

Claims 1, 4-6, 8, 10, 11, 13, 14, and 17-19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over DeRoo in view of Corrigan.

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Claims 2, 3, 7, 9, 12, 15, 16, and 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over DeRoo in view of Corrigan and Baxter.

PRINCIPLES OF LAW

“What matters is the objective reach of the claim. If the claim extends to what is obvious, it is invalid under § 103.” *KSR Int’l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1742 (2007). To be nonobvious, an improvement must be “more than the predictable use of prior art elements according to their established functions.” *Id.* at 1740. Appellants have the burden on appeal to the Board to demonstrate error in the Examiner’s position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) (“On appeal to the Board, an applicant can overcome a rejection [under § 103] by showing insufficient evidence of *prima facie* obviousness or by rebutting the *prima facie* case with evidence of secondary indicia of nonobviousness.”) (quoting *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)). Therefore, we look to Appellants’ Briefs to show error in the proffered *prima facie* case.

ANALYSIS

Independent claims 1 and 13

After considering the evidence before us, and the respective arguments on both sides, it is our view that the DeRoo and Corrigan references fall short of rendering obvious Appellants’ claims 1 and 13. In the rejection, the Examiner relies on the secondary Corrigan reference for

purportedly teaching the claimed verification interface (Ans. 5). Appellants contend that the cited combination of DeRoo and Corrigan does not show the claimed “verification interface” (App. Br. 16). Specifically, Appellants aver that Corrigan does not show a verification interface where accesses *directed towards the system memory* are passed to said system memory in a *normal mode* and wherein accesses *directed towards the system memory* are passed to said *shared memory* in a *verification mode* (App. Br. 16). In the Reply Brief, Appellants further point out that Corrigan teaches the use of two paths to the same memory (i.e., shared memory 202, Fig. 2), and thus does not show a verification interface that can pass system memory access to either one of two memories responsive to a signal (Reply Br. 3).

In the response to arguments section of the Answer, the Examiner apparently looks to the primary DeRoo reference for teaching the claimed system memory that is missing from Corrigan. Specifically, the Examiner contends that

the combination of DeRoo and Corrigan teaches the verification interface as Corrigan supplements the teachings of DeRoo by clearly teaching communications from a device on a first bus to a device on a second bus in a normal mode and communications from a device on a first bus to a device on a second bus that are directed to a shared memory in a loopback (or verification) mode.
(Ans. 14).

Regarding independent claims 1 and 13, it is our view that the weight of the evidence supports the Appellants’ position. Contrary to the Examiner’s position, we find that *both* the normal and loopback modes

taught by Corrigan are directed to a single shared memory 202 (*see* Figs. 2 and 3). In particular, Corrigan expressly discloses a first *normal mode* of operation that uses the direct connection between primary bus master 200 and shared memory 202, as shown in Figures 2 and 3, and further described as follows:

As shown in FIGS. 2 and 3, primary bus master 200 is directly connected to shared memory 202 via primary PCI bus 252. This connection is used in *normal operation* for the bus master to access the shared memory independent of the bridge circuit 206. In loopback mode operation, the primary bus master 200 uses its direct connection to shared memory 202 to verify proper operation of the loopback mode transactions with shared memory 202 via bridge circuit 206.

(Corrigan, col. 6, ll. 41-48, emphasis added).

As further disclosed by Corrigan, the loopback mode of operation routes data through bridge circuit 206 to shared memory 202, as shown in Figure 2, or alternately, in a reverse direction from shared memory 202 back through bridge circuit 206 to primary bus master 200, as shown in Figure 3 (*see also* Corrigan, col. 6, ll. 6-26). Therefore, we agree with Appellants that Corrigan teaches the use of two paths to the *same memory* (i.e., shared memory 202, Fig. 2).

Because the primary DeRoo reference merely shows two processors (CPU 702 and SCP 706) that may each read or write data to a common memory device 704, we conclude that DeRoo fails to remedy the deficiencies of Corrigan (*see* DeRoo, Fig. 20). We note that independent claim 13 recites the identical “verification interface” as recited in claim 1:

a verification interface for selectively passing system memory accesses either to the system memory or the shared memory responsive to the signal, wherein accesses directed towards the system memory access are passed to said system memory in a normal mode and wherein accesses directed towards the system memory are passed to said shared memory in a verification mode.

(Claims 1 and 13).

Because we conclude that Appellants have met their burden of showing that the Examiner has failed to establish a *prima facie* case of obviousness, we reverse the Examiner's rejection of independent claims 1 and 13 as being unpatentable over DeRoo in view of Corrigan. Since each associated dependent claim includes all the limitations of the claims from which it depends, we also reverse the Examiner's rejections of dependent claims 2-7 (that depend upon independent claim 1), and dependent claims 14-20 (that depend upon independent claim 13).

Independent claim 8

Initially, we note that Appellants have presented no arguments directed to the combinability of DeRoo and Corrigan with each other. Accordingly, Appellants have waived any such arguments, and the combinability of the references will not be addressed here.

While Appellants' arguments in the Briefs are primarily focused on the verification interface recited in each of independent claims 1 and 13, we note that broader language of independent claim 8 does not include the

aforementioned *verification interface*. Instead, independent claim 8 more broadly recites the steps of:

selectively passing system memory accesses to said system memory in a normal mode; and

selectively passing system memory accesses to said shared memory in a verification mode.

(claim 8).

It is our view that DeRoo teaches selectively passing system memory accesses (i.e., from either of CPU 702 or SCP 706) to the “system” memory (i.e., common memory device 704) in a “normal” mode (*see* DeRoo, Fig. 20, and associated discussion col. 37, ll. 6-22). Thus, common memory device 704 is accessible by both the “master” processor (e.g., CPU 702) and the “slave” processor (e.g., SCP 706), as claimed (via the address and data buses shown Fig. 20 of DeRoo).

Corrigan clearly teaches memory accesses to a shared memory in a loopback (i.e., verification) mode, as discussed *supra* regarding claims 1 and 13. Because the Examiner’s rejection is based on the combination of DeRoo and Corrigan, we find the claimed steps of selective redirection of memory accesses would have been well within the level of knowledge and creativity possessed by a person of ordinary skill in the art, having the benefit of the teachings of DeRoo and Corrigan.¹

¹ Courts should “take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” *KSR*, 127 S. Ct. at 1741.

While we have acknowledged *supra* that the Examiner’s proffered combination of DeRoo and Corrigan does not teach or fairly suggest the *verification interface* of claims 1 and 13, we note again that a dedicated “verification interface” is not claimed in broader independent claim 8.

Because DeRoo discloses that one CPU always has the highest priority (col. 2, ll. 15-17), we see no error in the Examiner’s findings regarding the claimed master and slave processors and associated subsystems (*see Ans.* 11). Moreover, it is our view that Corrigan necessarily teaches a signal (or signals) indicative of a normal mode of operation, or a loopback mode of operation (i.e., verification mode). See e.g., the discussion of enabling the loopback operation mode at column 3, lines 4-9.

Regarding the claimed external memory interface, Appellants merely state that “the slave processor [as claimed] has an external memory interface allowing access to the system memory.” (*See App. Br.* 15, ¶4, last sentence). A statement which merely points out what the claim recites does not satisfy Appellants’ burden to show error in the Examiner’s *prima facie* case.

Therefore, for at least the aforementioned reasons, we find the combination of DeRoo and Corrigan reasonably teaches and/or suggests the much broader limitations of independent claim 8 that were not squarely addressed by Appellants in the Briefs. Accordingly, we sustain the Examiner’s rejection of independent claim 8 as being unpatentable over DeRoo in view of Corrigan.

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Dependent claims 9-12

Appellants have not presented any substantive arguments directed separately to the patentability of the claims 9-12 that depend from independent claim 8. In the absence of a separate argument with respect to those claims, they stand or fall with the representative independent claim. *See In re Young*, 927 F.2d 588, 590 (Fed. Cir. 1991). Therefore, we sustain the Examiner's rejections of dependent claims 9-12.

CONCLUSION OF LAW

Based on the findings of facts and analysis above, we conclude that Appellants have met their burden of showing that the Examiner erred in rejecting claims 1-7 and 13-20 under 35 U.S.C. § 103(a) for obviousness.

However, we conclude that Appellants have not met their burden of showing that the Examiner erred in rejecting claims 8-12 under 35 U.S.C. § 103(a) for obviousness.

DECISION

We reverse the Examiner's decision rejecting claims 1-7 and 13-20 under 35 U.S.C. § 103(a) for obviousness.

We affirm the Examiner's decision rejecting claims 8-12 under 35 U.S.C. § 103(a) for obviousness.

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No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

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